# DESCRIPTION

## INVERTER DEVICE

### TECHNICAL FIELD

[0001] The present invention relates to an inverter device, more specifically to an inverter device including a circuit for preventing compression destruction and malfunction of a high compression integrated circuit (IC) that performs drive control of an inverter circuit provided with a switching element for driving load.

### BACKGROUND ART

[0002] In a conventional inverter device, as a countermeasure for a negative surge that is generated due to an amount of change of current (di/dt) per unit time and inductance of wiring when a switching element that drives load switches, a technology for connecting a clamp diode between a low pressure side reference terminal and a high pressure side reference terminal of a high compression IC that performs drive control of the switching element is disclosed (refer to Patent Document 1).

[0003] The technology disclosed in Patent Document 1 prevents destruction of the high compression IC by clamping, with the clamp diode, a negative voltage that occurs due to a slight inductance such as a chip pattern or wiring that causes destruction of the high compression IC.

[0004] In addition to the clamp diode disclosed in Patent Document 1, an example of a configuration of an inverter device provided with a voltage dividing circuit (resistance element) connected in series with the clamp diode is disclosed (refer to Patent Document 2).

[0005] In the technology disclosed in Patent Document 2,

negative voltage applied to the high compression IC is reduced by dividing the negative voltage, which cannot be suppressed only by the clamp diode, with the clamp diode and the resistance element of the voltage dividing circuit.

[0006] [Patent Document 1] Japanese Patent Application Laid Open No. H10-42575

[Patent Document 2] Japanese Patent No. 3577478

## DISCLOSURE OF INVENTION

### PROBLEM TO BE SOLVED BY THE INVENTION

[0007] However, in the conventional technology disclosed in Patent Document 1, the clamp diode and a diode connected back-to-back to the switching element of a lower arm (diode for flowing circulating current) are connected in parallel, and therefore, there is a possibility that the circulating current will flow in the clamp diode itself. Accordingly, a diode of a large current rating needs to be employed (a diode of a substantially same rating as the back-to-back connected diode), which directly leads to increases in cost and size.

[0008] On the other hand, in the conventional technology disclosed in Patent Document 2, there is a possibility that a circulating current will flow into both the clamp diode and the voltage dividing circuit. Accordingly, similarly to the conventional technology disclosed in Patent Document 1, both a diode of a large current rating and a resistance element need to be employed, and therefore, the disadvantage of increases in cost and size cannot be avoided.

[0009] A typical high compression IC includes an input buffer, a metal-oxide (MOS) transistor, a resistor, a driver circuit, and so forth. Thus, when a negative voltage is generated, a through current flows through

parasitic capacity of the MOS transistor into the high compression IC. A latch up phenomenon, in which the driver circuit in the high compression IC outputs an erroneous signal, is caused by the through current. The conventional technologies disclosed in Patent Documents 1 and 2 are insufficient for solving the problem of the latch up.

[0010] The present invention has been made in view of the above, and an object of the present invention is to provide an inverter device that can prevent destruction and malfunction (latch up) of a high compression IC for controlling an inverter circuit, and providing circuit technology that can suppress increases in circuit scale and cost.

MEANS FOR SOLVING PROBLEM

[0011] To solve the above problems and to achieve the above object, an inverter device according to an aspect of the present invention includes an inverter circuit including a bridge circuit connected between a positive electrode and a negative electrode of a direct current power supply, the bridge circuit including an upper arm unit and a lower arm unit connected in series, wherein the upper arm unit includes a upper arm switching element and a diode connected back-to-back to each other, and the lower arm unit includes a lower arm switching element and a diode connected back-to-back to each other; an inverter driving unit including a high compression IC that drives the upper arm switching element and the lower arm switching element; and a clamp unit that clamps a difference in potential between a lower-arm driving reference supply terminal of the high compression IC and an upper arm driving high-pressure side power supply terminal of the high compression IC.

[0012] According to the above aspect, a clamping means for clamping a difference in potential between a lower arm driving reference supply terminal of a high compression IC and an upper arm driving high-pressure side power supply terminal of the high compression IC clamps a negative voltage that causes compression destruction in the high compression IC due to wiring inductance and circulating current, and reduces through current flowing inside the high compression IC.

EFFECT OF THE INVENTION

[0013] According to an inverter device of the present invention, a clamping means for clamping a difference in potential between a lower arm driving reference supply terminal of a high compression IC and an upper arm driving high-pressure side power supply terminal of the high compression IC clamps a negative voltage that causes compression destruction in the high compression IC, and prevents a large portion of through current from flowing inside the high compression IC. Therefore, destruction and malfunction (latch up) of the high compression IC can be prevented, and increases in circuit scale and cost can be suppressed.

BRIEF DESCRIPTION OF DRAWINGS

[0014] Fig. 1 is a schematic for explaining an inverter device (single-phase inverter configuration) according to a first embodiment of the present invention.

Fig. 2 is a schematic for describing malfunction of a high compression IC in an inverter device in which a clamp diode is not connected.

Fig. 3 is a schematic for describing a state in which through current flowing toward a high compression IC is

drawn to a side of a clamp diode in the inverter device according to the first embodiment.

Fig. 4 is a schematic for explaining an inverter device (three-phase inverter configuration: independent power supply) according to a second embodiment of the present invention.

Fig. 5 is a schematic for explaining an inverter device (three-phase inverter configuration: common power supply) according to a third embodiment of the present invention.

EXPLANATIONS OF LETTERS OR NUMERALS

[0015]

2, 2a inverter driving unit
3, 3a inverter circuit
4, 4a, 4b, 4c upper arm unit
5, 5a, 5b, 5c lower arm unit
6, 6a bridge circuit
7 DC power supply
8 load
10, 10a high compression IC
12 driver circuit
14 input buffer
16 NMOS transistor
17 parasitic diode
20 resistor
C1, C2, C3, C5 decoupling condenser
D1, D3, D5 upper arm diode
D2, D4, D6 lower arm diode
D10, D11, D12, D13, D21, D22, D23 clamp diode
D17 parasitic diode
R1, R2, R3, R4, R5, R6 gate resistor
T1, T3, T5 upper arm switching element

T2, T4, T6 lower arm switching element

BEST MODE(S) FOR CARRYING OUT THE INVENTION

[0016] Exemplary embodiments of an inverter device according to the present invention will be described below with reference to accompanying drawings. The present invention is not limited to these embodiments.

[0017]First Embodiment

Fig. 1 is a schematic for explaining an inverter device according to a first embodiment of the present invention. The inverter device employs a configuration of a typical single-phase inverter device, in which an inverter driving unit 2 including a high compression IC 10 drives a switching element T1 in an upper arm and a switching element T2 in a lower arm of an inverter circuit 3. The inverter device according to the first embodiment is described with reference to Fig. 1.

[0018] In the inverter circuit 3 shown in Fig. 1, an upper arm unit 4 including the switching element (upper arm switching element) T1 in the upper arm and a diode (upper arm diode) D1 connected back-to-back to each other, and a lower arm unit 5 including the switching element (lower arm switching element) T2 in the lower arm and a diode (lower arm diode) D2 connected back-to-back to each other, are connected in series in a bridge circuit 6. A positive electrode of a DC power supply 7 of the bridge circuit 6 is connected to a corrector of the upper arm switching element T1, and a negative electrode of the DC power supply 7 is connected to an emitter of the lower arm switching element T2. Thus, the inverter circuit 3 shown in Fig. 1 has a configuration of a single-phase inverter circuit.

[0019] The high compression IC 10 of the inverter driving unit 2 shown in Fig. 1 drives the upper arm

switching element T1 and the lower arm switching element T2 in the inverter circuit 3. The high compression IC 10 includes input/output terminals described below. Specifically, the terminals are a VDD that is a high-pressure side power supply terminal for controlling the high compression IC 10, a COM that is a reference supply for controlling the high compression IC 10, an upper arm control signal input terminal HIN to which a control signal for controlling the upper arm unit 4 is input, a lower arm control signal input terminal LIN to which a control signal for controlling the lower arm unit 5 is input, an upper arm driving high-pressure side power supply terminal VB connected to a high pressure side of a driving power supply that drives the upper arm unit 4, an upper arm driving reference supply terminal VS that is a reference terminal of the driving power supply that drives the upper arm unit 4, an upper arm switching element driving signal output terminal HO from which a driving signal for driving the upper arm unit 4 is output, a lower arm driving high-pressure side power supply terminal VCC that is connected to a high-pressure side of a driving power supply that drives the lower arm unit 5, a lower arm driving reference supply terminal COM that is a reference terminal of the driving power supply that drives the lower arm unit 5, and a lower arm switching element driving signal output terminal LO from which a driving signal for driving the lower arm unit 5 is output.

[0020] A decoupling condenser C1 is connected between the upper arm driving high-pressure side power supply terminal VB and the upper arm driving reference supply terminal VS. A decoupling condenser C2 is connected between the lower arm driving high-pressure side power supply terminal VCC and the lower arm driving reference

supply terminal COM.

[0021] In between the inverter circuit 3 and the high compression IC 10, a gate resistor R1 that controls gate current connects the upper arm switching element driving signal output terminal HO and a gate of the upper arm switching element T1. The upper arm driving reference supply terminal VS and an emitter of the upper arm switching element T1 are directly connected. Similarly, a gate resistor R2 connects the lower arm switching element driving signal output terminal LO and a gate of the lower arm switching element T2. The lower arm driving reference supply terminal COM and the emitter of the lower arm switching element T2 are directly connected.

[0022] In the inverter device shown in Fig. 1, wiring inductance is minimized as much as possible by, for example, connecting the upper arm switching element T1 and the lower arm switching element T2 with a plurality of wires (wire bunch), directly connecting these switching elements and output terminals by bonding pads without using wires, and separating a corrector and an emitter of each switching element onto a front surface and a back surface of a substrate. A composite inductance L11 shown between the emitter of the lower arm switching element T2 of the inverter circuit 3 and the lower arm driving reference supply terminal COM of the high compression IC 10 indicates composite inductance in a circuit part including the lower arm diode D2 through which circulating current flows. The composite inductance L11 is suppressed between a few nH to few dozens of nH by the aforementioned measures.

[0023] The circulating current flows for a short period of time, and an amount of change of current (di/dt) per unit time is large, and therefore, even if the composite inductance of the circuit part where circulating current

flows is small, a few voltages of some inductive voltages are generated. The polarity of the inductive voltage is a negative voltage. Specifically, when the potential of the lower arm driving reference supply terminal COM is the reference, the potential of the upper arm driving reference supply terminal VS is negative. Accordingly, compression destruction occurs in the high compression IC. Moreover, the negative voltage causes latch up, i.e., the driver circuit of the high compression IC 10 outputs an erroneous signal.

[0024] The inverter device according to the first embodiment shown in Fig. 1 includes a clamp diode D10 as a clamping means for clamping a difference in potential between the lower arm driving reference supply terminal COM and the upper arm driving high-pressure side power supply terminal VB to a predetermined voltage. An anode of the clamp diode D10 is connected to the lower arm driving reference supply terminal COM, and a cathode of the clamp diode D10 is connected to the upper arm driving high-pressure side power supply terminal VB. The position at which the clamp diode D10 is connected in the is different from the positions of the clamp diodes disclosed in Patent Documents 1, 2, the reason of which will be described below.

[0025] The reason why the clamp diode D10 is connected between the lower arm driving reference supply terminal COM and the upper arm driving high-pressure side power supply terminal VB as shown in Fig. 1, is described with reference to Figs. 2 and 3. Fig. 2 is a schematic for describing malfunction of a high compression IC in an inverter device in which a clamp diode is not connected, and Fig. 3 is a schematic for describing a state in which through current flowing toward a high compression IC is drawn to a side of the clamp diode in the inverter device according to the

first embodiment.

[0026] Fig. 2 is a detailed schematic of an inside of the high compression IC 10 shown in Fig. 1. In Fig. 2, the high compression IC 10 includes an input buffer 14, an N-channel metal oxide (NMOS) transistor 16, a parasitic diode 17, a resistor 20, and a driver circuit 12. An input terminal of the input buffer 14 is connected to the upper arm control signal input terminal HIN, and an output terminal of the input buffer 14 is connected to a gate of the NMOS transistor 16. The parasitic diode 17 is connected to the NMOS transistor 16 in parallel. A corrector of the NMOS transistor 16 is connected to an input terminal of the driver circuit 12, and connected to the upper arm driving high-pressure side power supply terminal VB through the resistor 20 that is connected to the input terminal of the driver circuit 12.

[0027] A mechanism of a malfunction of the high compression IC is described next. In Fig. 2, when the upper arm switching element T1 is turned on, a main circuit current I1 indicated by a wavy line flows in a load 8 that has an inductance component. When the upper arm switching element T1 is turned off, the current flowing in the load 8 flows through the lower arm diode D2 as a circulating current I2 having an acute inclination and into the load 8. As described above, components in the inverter circuit 3 are connected by patterns and wires, and a slight inductor component is present between the components. Among these inductance components, a position of an inductance component where the circulating current I2 flows is denoted by L11. Assuming that an inductive voltage VL is generated in the inductance component L11 when the circulating current I2 flows through, the inductive voltage VL can be expressed by the following equality.

[0028]

$$VL=L11\times(di/dt) \quad (1)$$

[0029] As the impedance of the load 8 decreases, inclination of a current flow becomes more acute (specifically, di/dt in the equality (1) increases), so that the inductive voltage VL increases.

[0030] Furthermore, an on voltage VF is generated in the lower arm diode D2 when the circulating current I2 flows. Thus, a difference in potential occurs between the emitter of the upper arm switching element T1 and the emitter of the lower arm switching element T2, as expressed by the following equality:

[0031]

$$\Delta V=VL+VF \quad (2)$$

[0032] The emitter of the upper arm switching element T1 and the emitter of the lower arm switching element T2 are connected to the upper arm driving reference supply terminal VS and the lower arm driving reference supply terminal COM of the high compression IC 10, respectively. Therefore, a voltage $\Delta V$ expressed by the equality (2) is applied between these terminals.

[0033] The high compression IC 10 includes the input buffer 14, the NMOS transistor 16, the parasitic diode 17, the resistor 20, and the driver circuit 12, and therefore, when $\Delta V1$ is applied, a through current I3 flows from the parasitic diode 17 through the resistor 20. The through current I3 mainly causes the driver circuit 12 to output an erroneous signal, called the latch up phenomenon.

[0034] The inverter device according to the first embodiment includes the clamp diode D10 provided between the lower arm driving reference supply terminal COM and the upper arm driving high-pressure side power supply terminal

VB, and therefore, the through current I3 flowing inside the high compression IC 10 in the circuit configuration shown in Fig. 2 can be drawn to the clamp diode D10 side as shown in Fig. 3. Part of the through current might flow in the high compression IC 10, however, an impedance in the clamp diode D10 connected between the same terminal is smaller than an impedance in a series circuit of a parasitic diode D17 and the resistor 20 through which the through current I3 flows. Therefore, a large portion of the through current I3 can be drawn to the clamp diode D10 side, so that the through current I3 that flows inside the high compression IC 10 can be reduced, and malfunction caused by latch up can be prevented.

[0035] In the inverter device disclosed in patent documents 1, 2, one terminal (cathode) of the clamp diode is connected to the upper arm driving reference supply terminal VS. Thus, the conventional clamp diode cannot draw the through current as much as the clamp diode D10 of the first embodiment.

[0036] The inverter device according to the first embodiment, the cathode of the clamp diode D10 is connected to the upper arm driving high-pressure side power supply terminal VB (for example +15V terminal) of the high compression IC 10, and therefore, the current flowing through the clamp diode D10 can be reduced compared to the current flowing through the clamp diode disclosed in Patent Documents 1, 2. Therefore, a diode of a smaller current rating compared to the clamp diode disclosed in Patent Documents 1, 2 can be employed in the first embodiment.

[0037] As described above, in the inverter device according to the first embodiment, the clamp diode connected between the lower arm driving reference supply terminal of the high compression IC and the upper arm

driving high-pressure side power supply terminal of the high compression IC clamps a difference in potential between the lower arm driving reference supply terminal and the upper arm driving high-pressure side power supply terminal. Therefore, destruction and malfunction of the high compression IC is prevented, and increases in circuit scale and cost is suppressed.

[0038] In the first embodiment, the clamp diode is attached on the outside of the high compression IC, but the clamp diode can be attached on the inside of the high compression IC. However, it is advantageous to attach the clamp diode on the outside of the high compression IC, because it is not necessary to change the design of the high compression IC, and the present invention can be applied to an inverter device employing an existing high compression IC.

[0039] Furthermore, in the first embodiment, a diode is used as the clamping means for clamping a difference in potential between the lower arm driving reference supply terminal and the upper arm driving high-pressure side power supply terminal, however, the clamping means is not limited to the diode. Any element that turns on at a certain voltage and outputs a substantially constant voltage can be used, such as a zener diode or a PN junction of a bipolar transistor.

[0040]Second Embodiment

Fig. 4 is a schematic for explaining an inverter device according to a second embodiment of the present invention. The inverter device according to the first embodiment included a single-phase inverter circuit, whereas the inverter device according to second embodiment includes a three-phase inverter circuit. The inverter device shown in Fig. 4 employs a configuration of a typical

three-phase inverter device, in which an inverter driving unit 2a including a high compression IC 10a drives upper arm switching elements T1, T3, T5 and lower arm switching elements T2, T4, T6 of an inverter circuit 3a. The inverter device according to the second embodiment is described with reference to Fig. 4. The components in the second embodiment that perform same or similar function or that have same or similar configuration as those in the first embodiment are denoted by the same reference numerals as in the first embodiment, and overlapping descriptions are omitted.

[0041] The inverter circuit 3a shown in Fig. 4 includes an upper arm unit 4a including the upper arm switching element T1 and the upper arm diode D1 connected back-to-back to each other, an upper arm unit 4b including the upper arm switching element T3 and an upper arm diode D3 connected back-to-back to each other, an upper arm unit 4c including the upper arm switching element T5 and an upper arm diode D5 connected back-to-back to each other, a lower arm unit 5a including the lower arm switching element T2 and a lower arm diode D2 connected back-to-back to each other, a lower arm unit 5b including the lower arm switching element T4 and a lower arm diode D4 connected back-to-back to each other, and a lower arm unit 5c including the lower arm switching element T6 and a lower arm diode D6 connected back-to-back to each other. Each of the back-to-back connection circuits, the upper arm units 4a, 4b, 4c, are connected in series to each of the back-to-back connection circuits, the lower arm units 5a, respectively, in a bridge circuit 6a. In the bridge circuit 6a, the positive electrode of the DC power supply 7 is connected to each corrector of the upper arm switching elements T1, T3, T5, and the negative electrode of the DC

power supply 7 is connected to each emitter of the lower arm switching elements T2, T4, T6. Thus, the inverter circuit 3a shown in Fig. 4 has a configuration of a three-phase inverter circuit.

[0042] The high compression IC 10a in the inverter driving unit 2a shown in Fig. 4 drives the upper arm switching elements T1, T3, T5 and the lower arm switching elements T2, T4, T6 in the inverter circuit 3a. The high compression IC 10a includes input/output terminals described below. Specifically, the terminals are the high-pressure side power supply terminal for control VDD, the reference supply for control COM, the upper arm control signal input terminal HIN, the lower arm control signal input terminal LIN, upper arm driving high-pressure side power supply terminals VB1, VB3, VB5, upper arm driving reference supply terminals VS1, VS3, VS5, upper arm switching element driving signal output terminals HO1, HO3, HO5, the lower arm driving high-pressure side power supply terminal VCC, the lower arm driving reference supply terminal COM, and lower arm switching element driving signal output terminals LO2, LO4, LO6.

[0043] Decoupling condensers C1, C3, C5 are connected between each terminal of the upper arm driving high-pressure side power supply terminals VB1, VB3, VB5 and each terminal of the upper arm driving reference supply terminals VS1, VS3, VS5, respectively. The decoupling condenser C2 is connected between the lower arm driving high-pressure side power supply terminal VCC and the lower arm driving reference supply terminal COM.

[0044] In between the inverter circuit 3a and the high compression IC 10a, each terminal of the upper arm switching element driving signal output terminals HO1, HO3, HO5 and each gate of the upper arm switching elements T1,

T3, T5 are connected by gate resistors R1, R3, R5, respectively. Each terminal of the upper arm driving reference supply terminals VS1, VS3, VS5 is directly connected to each emitter of the upper arm switching elements T1, respectively. Similarly, each terminal of the lower arm switching element driving signal output terminals LO1, HO3, HO5 and each gate of the lower arm switching elements T2, T4, T6 are connected by gate resistors R2, R4, R6, respectively. The lower arm driving reference supply terminal COM is directly connected to each emitter of the lower arm switching elements T2.

[0045] The inverter device according to the second embodiment includes clamp diodes D11, D12, D13 as clamping arrangement for clamping a difference in potential between the lower arm driving reference supply terminal COM and each terminal of the upper arm driving high-pressure side power supply terminals VB1, VB3, VB5 to a predetermined voltage. Each anode of the clamp diodes D11, D12, D13 is connected to the lower arm driving reference supply terminal COM, and each cathode of the clamp diodes D11, D12, D13 is connected to each terminal of the upper arm driving high-pressure side power supply terminals VB1, VB3, VB5, respectively.

[0046] Thus, in the inverter device according to the second embodiment, similarly to the first embodiment, a large portion of through current flowing toward the inside of the high compression IC 10a can be drawn to the side of the clamp diodes D11, D12, D13, so that the through current that flows toward the high compression IC 10 can be reduced, and malfunction caused by latch up can be prevented.

[0047] Furthermore, in the inverter device according to the second embodiment, each cathode of the clamp diodes D11, D12, D13 is connected to each terminal of the upper arm

driving high-pressure side power supply terminals VB1, VB3, VB5, respectively. Therefore, current flowing through the clamp diodes D11, D12, D13 can be reduced compared to current flowing through the clamp diode disclosed in Patent Documents 1, 2. Accordingly, a diode of a smaller current rating compared to the clamp diode disclosed in Patent Documents 1, 2 can be employed in the second embodiment.

[0048] As described above, the inverter device according to the second embodiment, each clamp diode connected between each terminal of the lower arm driving reference supply terminal of the high compression IC and each terminal of the upper arm driving high-pressure side power supply terminal of the high compression IC, respectively, clamps each difference in potential between the lower arm driving reference supply terminal and each terminal of the upper arm driving high-pressure side power supply terminal. Therefore, destruction and malfunction of the high compression IC is prevented, and increases in circuit scale and cost is suppressed.

[0049] In the second embodiment, each clamp diode is attached on the outside of the high compression IC, but the clamp diode can be attached on the inside of the high compression IC. However, it is advantageous to attach the clamp diode on the outside of the high compression IC, because it is not necessary to change the design of the high compression IC, and the present invention can be applied to an inverter device employing an existing high compression IC.

[0050] Furthermore, in the second embodiment, a diode is used as the clamping arrangement for clamping each difference in potential between the lower arm driving reference supply terminal and each terminal of the upper arm driving high-pressure side power supply terminal,

however, the clamping arrangement is not limited to the diode. Any element that turns on at a certain voltage and outputs a substantially constant voltage can be used, such as a zener diode or a PN junction of a bipolar transistor.

[0051]Third Embodiment

Fig. 5 is a schematic for explaining an inverter device according to a third embodiment of the present invention. The inverter device according to the second embodiment includes independent power supplies for individually driving each switching element in the upper arm unit, and a common power supply for driving each switching element in the lower arm unit, whereas in the inverter device according to the third embodiment, each switching element in the upper and lower arm units are driven by a common power supply. Therefore, a connection configuration of the clamp diodes is different from that of the second embodiment. The components in the third embodiment that perform same or similar function or that have same or similar configuration as those in the second embodiment are denoted by the same reference numerals as in the first embodiment, and overlapping descriptions are omitted.

[0052] The inverter device according to the third embodiment shown in Fig. 5 includes a first clamp diode D10 and second clamp diodes D21, D22, D23 as clamping arrangement for clamping a difference in potential between the lower arm driving reference supply terminal COM and each terminal of the upper arm driving high-pressure side power supply terminals VB1, VB3, VB5 to a predetermined voltage. An anode of the first clamp diode D10 is connected to the lower arm driving reference supply terminal COM, and a cathode of the first clamp diode D10 is connected to the lower arm driving high-pressure side power

supply terminal VCC. Each anode of the second clamp diodes D21, D22, D23 is connected to the lower arm driving high-pressure side power supply terminal VCC, and each cathode of the second clamp diodes D21, D22, D23 is connected to each terminal of the upper arm driving high-pressure side power supply terminals VB1, VB3, VB5, respectively.

[0053] Thus, in the inverter device according to the third embodiment, similarly to the inverter devices according to the first and second embodiments, a large portion of through current flowing toward the inside of the high compression IC 10a can be drawn to the side of the first clamp diode D10 and the second clamp diodes D11, D12, D13, so that the through current that flows toward the inside the high compression IC 10 can be reduced, and malfunction caused by latch up can be prevented.

[0054] Furthermore, in the inverter device according to the third embodiment, each cathode of the second clamp diodes D21, D22, D23 is connected to each terminal of the upper arm driving high-pressure side power supply terminals VB1, VB3, VB5, respectively. Therefore, current flowing through the second clamp diodes D21, D22, D23 can be reduced compared to current flowing through the clamp diode disclosed in Patent Documents 1, 2. Therefore, a diode of a smaller current rating compared to the clamp diode disclosed in Patent Documents 1, 2 can be employed in the third embodiment.

[0055] As described above, in the inverter device according to the third embodiment, the first clamp diode connected between the lower arm driving reference supply terminal of the high compression IC and the lower arm driving high-pressure side power supply terminal of the high compression IC, and the second clamp diodes connected between the lower arm driving high-pressure side power

supply terminal of the high compression IC and each terminal of the upper arm driving high-pressure side power supply terminals of the high compression IC clamp each difference in potential between the lower arm driving reference supply terminal and each terminal of the upper arm driving high-pressure side power supply terminals. Therefore, destruction and malfunction of the high compression IC is prevented, and increases in circuit scale and cost is suppressed.

[0056] In the third embodiment, each clamp diode is attached on the outside of the high compression IC, but the clamp diode can be attached on the inside of the high compression IC. However, it is advantageous to attach the clamp diode on the outside of the high compression IC, because it is not necessary to change the design of the high compression IC, and the present invention can be applied to an inverter device employing an existing high compression IC.

[0057] Furthermore, in the third embodiment, a diode is used as the clamping arrangement for clamping each difference in potential between the lower arm driving reference supply terminal and each terminal of the upper arm driving high-pressure side power supply terminal, however, the clamping arrangement is not limited to the diode. Any element that turns on at a certain voltage and outputs a substantially constant voltage can be used, such as a zener diode or a PN junction of a bipolar transistor.

INDUSTRIAL APPLICABILITY

[0058] As described above, an inverter device according to the present invention can be widely applied to an inverter device including, for example, a single-phase inverter circuit or a three-phase inverter circuit, and is

particularly suitable as an inverter device specifically required to prevent malfunction and compression destruction of a high compression IC.